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| 10/037,716 | 11/09/2001 | Xiaobao Wang | 9818-059-999 | 8298 |

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| EXAMINER | |
|---|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/037,716 | WANG ET AL. | |
| | Examiner | Art Unit | |
| | An T. Luu | 2816 | |

*-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *4-12-04 (RCE)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-28* is/are allowed.

6)☒ Claim(s) *1-10,12,15 and 29-37* is/are rejected.

7)☒ Claim(s) *11,13,14 and 16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-7, 10, 19 and 29-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 8-9, the limitation "the input/output supply signal for the logic device" lacks antecedent basis. It is noted that "the input/output supply signal for the logic device" is totally different from "input/output supply signal standard", lines 2-3, since figure 1 and page 5, lines 25-26 of the specification indicate that "the input/output supply signal for the logic device" is either VREF or VREF_CONTROL wherein "input/output supply signal standard" is one of Vcc, Pvcca, Pvccb, Ground, Pgnda, Pgndb.

In claim 10, line 2, the limitation "the first supply signal" lacks antecedent basis.

As to claim 29, on line 5, the limitation "supplying a dedicated supply signal to the logic device" appears to be misdescriptive since figure 1 shows "a dedicated supply signal" (VCC_DED) for determining when the VREF is supplying to the logic device. In other words, "a dedicated supply signal" is for turning ON/OFF switch 110 to pass "the VREF" to the logic device.

As to claim 37, the recitation of claims appears to be misdescriptive since figure 1 of the instant application shows transistor T5 being conducted and transistors T1 and T2 being non-

conducted as the same instant. Therefore, the dedicated supply signal (VCC_DED) is not providing to anything when transistor T5 is in conductive mode (i.e., shorting)

Claims 2-7, 19 and 30-36 are rejected for being dependent on the rejected claim as noted above.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10, 12, 15, 19 and 29-36, as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over the Miske reference (U.S. Patent 6,163,199).

Miske discloses in figure 8 an apparatus 12 for selectively providing a reference voltage signal (node A) to a logic device coupled to node B (not shown) operable in accordance with a plurality of input/output supply signal standards (Vcc, Pvcca, Pvccb, Ground, Pgnda, Pgndb) each having a specified input/output supply signal level, wherein at least one of the plurality of input/output supply signal standards is a voltage reference standard (Vcc), the switch circuit comprising a transmission switch circuit (M0, M1, M6, M7) receiving the reference voltage signal (node A) at an input thereof and passing the reference voltage signal to an output (node B) thereof in response to a first control signal (output of I17), the first control signal having a logic level determined by a dedicated supply signal (Pgndb) that is different from an input/output supply signal for the logic device as required by claim 1.

Miske does not disclose a logic device coupled to the output of the switching circuit as specifically required by claim.

It would have been obvious to one skilled in the art at the time the invention was made to provide a logic device at the output node of the circuit since the output of the inventive circuit is intended for further processing (See ABRACT and SUMMARY OF INVENTION).

A skilled artisan in the art would have been motivated to provide a logic circuit or any other device, at the output of the inventive circuit for the benefit of having a reliable process of transferring signals from input terminal to output terminal in an environment of having multiple operating supplied voltages (i.e., 5V, 3V or 2V).

As to claim 2, col. 7, lines 35-41, discloses GROUND potential is the lowest specified input/output supply signal level. Therefore, the dedicated supply signal level is greater than GROUND potential.

As to claim 3, figure 7 and col. 8, lines 29-30, discloses the dedicated supply voltage (Pgndb) having voltage level of 3 volts (i.e., higher than 2.5V).

As to claims 4 and 5, figure 8 shows the transmission switch circuit comprising an NMOS transistor M7 having a control terminal for receiving the first control signal (output of I17).

As to claim 6, figure 8 shows transistor M7 having source terminal coupled to the input (A) and drain terminal coupled to the output (B).

As to claim 7, figure 8 shows the transmission switch circuit comprising PMOS transistor M1 having gate terminal for receiving a second control signal (output of I15) complementary of

the first control signal (by means of inverter I13) wherein the PMOS and NMOS transistors being in parallel connection.

As to claim 19, Miske does not disclose a buffer coupled between the logic circuit and the transmission switch circuit as required by claim. It is well known in the art to one skilled in the art to utilize a buffer at input/output signal for achieving a desired signal level suitable for further processing. Thus, it would have been obvious to one skilled in the art to insert a buffer between the logic circuit and the transmission switch circuit to reshape the signal outputted from the switch circuit to a proper level which is suitable to the required operating level of the logic circuit along the processing line.

As to claim 8, the scope of claim is similar to that of claim 1. Therefore, it is rejected for the same reason set forth above. It is noted that inverter I17 is a first logic level shifting circuit receiving a master control signal (OEN) at an input thereof, the master control signal having a first logic level (either high or low, col. 2, lines 14-18), the first logic level shifting circuit further receiving the dedicated supply signal and providing the first control signal at an output thereof.

As to claim 9, figure 8 shows a second logic level shifting circuit (I15) receiving the master control signal (EON via I13) at an input thereof, the second logic level shifting circuit further receiving the input/output supply signal (Pvccb) and providing a second control signal at an output thereof.

As to claim 10, figure 8 shows when the master control signal is at the first logic level (i.e., low), the first control signal is at the logic level determined by the dedicated supply signal.

As to claim 12, the scope of claim is similar to that of claim 1. Therefore, it is rejected for the same reason set forth above. It is noted that figure 8 shows the transmission switch circuit

comprising first and second NMOS transistors (M6, M7) each having a gate terminal receiving the first control signal (OEN passing through I16 and I17)).

As to claim 15, figure 8 shows the transmission circuit comprising first and second PMOS transistors (M0, M1) each having a gate terminal for receiving a second control signal complementary to the first control signal (i.e., by means of inverter I13). Figure 8 further shows transistors M0 and M1 are in parallel with transistor M6 and M7.

As to claim 29, it is rejected for reciting a method derived from an apparatus of claim 1 or 8, as noted above.

As to claims 30 and 31, they are rejected for reciting a method derived from an apparatus of claims 10 and 11, respectively, as noted above.

As to claim 32, it is rejected for reciting a method derived from an apparatus of claim 7 as noted above.

As to claim 33, it is rejected for reciting a method derived from an apparatus recited in claim 1 or 8, as noted above.

As to claim 34, it is rejected for reciting a method derived from an apparatus of claim 3 as noted above.

As to claim 35, it is rejected as reciting result derived from an apparatus recited in claim 1 or 8, as noted above.

As to claim 36, it is rejected for reciting a method derived from an apparatus of claim 19 as noted above.

***Allowable Subject Matter***

5. Claims 20-28 are allowed.

6. Claims 11, 13-14 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claim 31 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claims. Specifically, none of the prior art, teaches or suggest, among other things, the following limitations:

- The master control signal is provided by a logic core of the logic device and the first logic level is determined by a core supply signal as required by claims 11 and 31.
- A source terminal of the first NMOS transistor provides the transmission switch circuit input, a drain terminal of the second NMOS transistor provides the transmission switch circuit output, and a drain terminal of the first NMOS transistor is coupled to the source terminal of the second NMOS transistor as required by claim 13.
- A first logic level shifting circuit receiving a master control signal at an input thereof, the master control signal having a logic level determined by a first supply signal, the first logic level shifting circuit further receiving the dedicated supply signal and

providing the first control signal at an output thereof; and a second logic level shifting circuit receiving the master control signal at an input thereof, the second logic level shifting circuit further receiving the input/output supply signal and providing the second control signal at an output thereof as required by claim 16.

- a source terminal of the first NMOS transistor and a source terminal of the first PMOS transistor provide the transmission switch circuit input, a drain terminal of the second NMOS transistor and a drain terminal of the second PMOS transistor provide the transmission switch circuit output, a drain terminal of the first NMOS transistor is coupled to the source terminal of the second NMOS transistor, and a drain terminal of the first PMOS transistor is coupled to the source terminal of the second PMOS transistor as required by claim 17.
- Structures of "a first logic level shifting circuit" and "a second level shifting circuit" as recited on lines 3-11 of claim 20.

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
5-6-04

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